

FIG. 1A

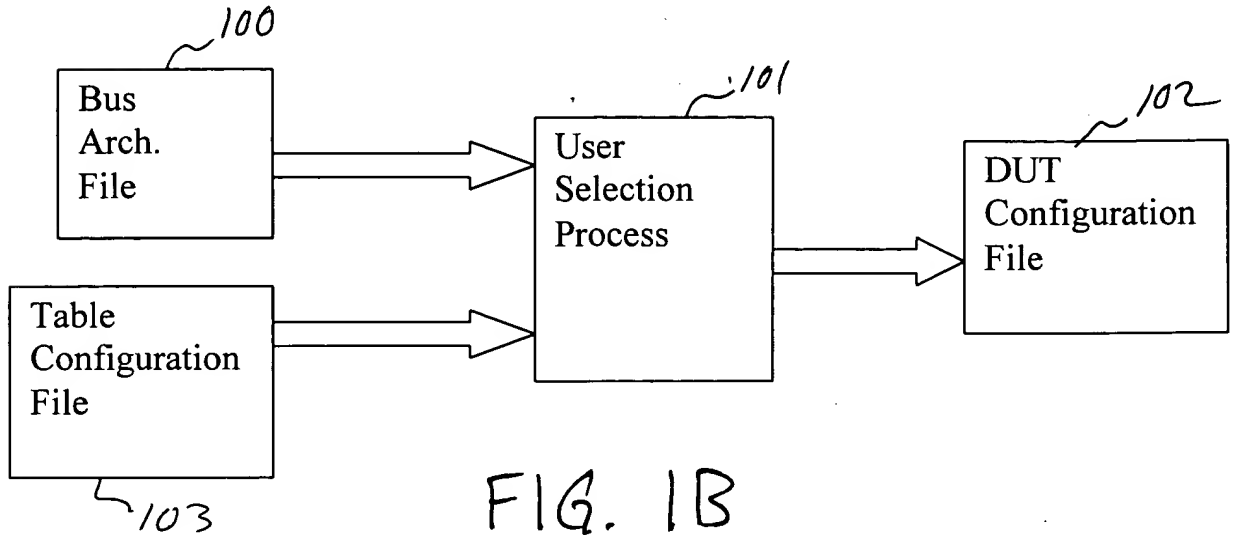


FIG. 1B

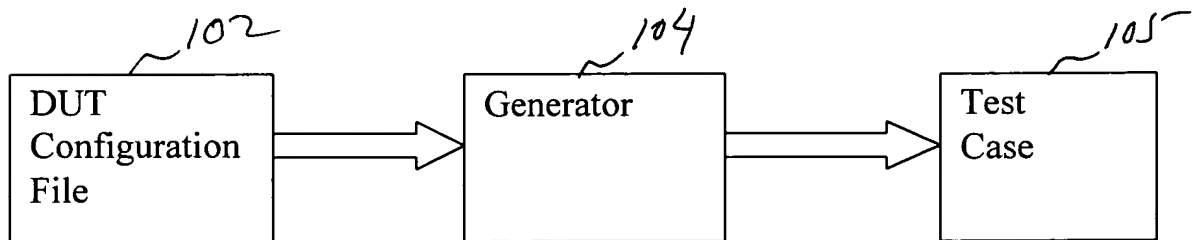


FIG. 1C

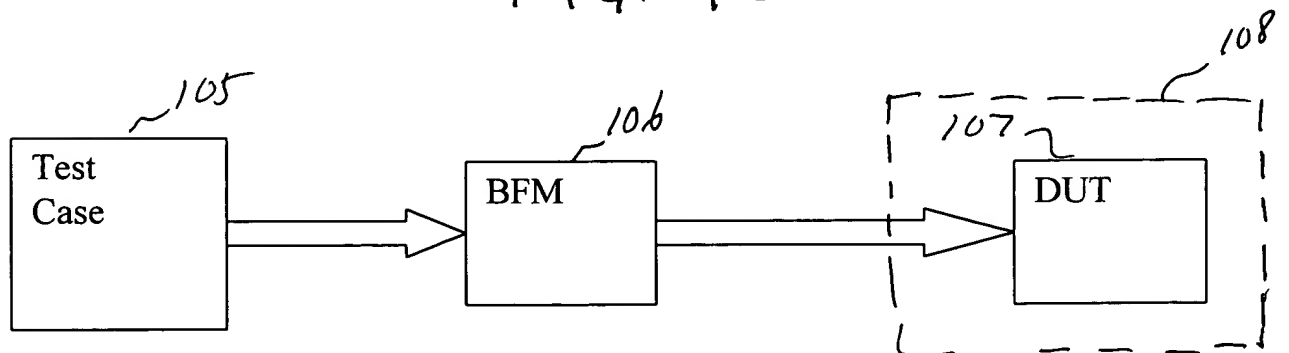


FIG. 1D

004T80" / 528E960

Address Range: to

☐ Single Transfers

☐ Burst Transfers

Burst Transfer Widths: ☐ byte ☐ half-word ☐ word ☐ double-word ☐ quad-word ☐

☐ Fixed-Length Burst Transfers

Fixed Burst Transfer Lengths: ☐ 2 ☐ 3 ☐ 4 ☐ 5 ☐ 6 ☐ 7 ☐ 8 ☐ 9 ☐ 10 ☐ 11 ☐

☐ Variable-Length Burst Transfers

Variable Burst Deassert Delay: to

☐ Line Transfers

Line Transfer Lengths: ☐ 4-word ☐ 8-word ☐ 16-word

Line Read Word Mode: ☐ sequential ☐ target word first

Master Data Bus Width: ☐ 32 ☐ 64 ☐ 128

Request Delay Range: to

Locked Transfers: ☒ locked ☐ unlocked ☒ both

Lock Deassert Delay: to

Transfer Types: ☐ memory ☐ plb slave buffered

Compressed Transfers: ☒ compressed ☒ non-compressed ☒ both

Guarded Transfers: ☒ guarded ☒ non-guarded ☒ both

Ordered Transfers: ☒ ordered ☒ non-ordered ☒ both

Lock Error Registers: ☒ lockerr ☒ non-lockerr ☒ both

Abort Transfers: ☒ abort ☒ non-abort ☒ both

Abort Assert Delay: to

Master Priority: ☐ 00 ☐ 01 ☐ 10 ☐ 11

FIG. 2

Best Available Copy

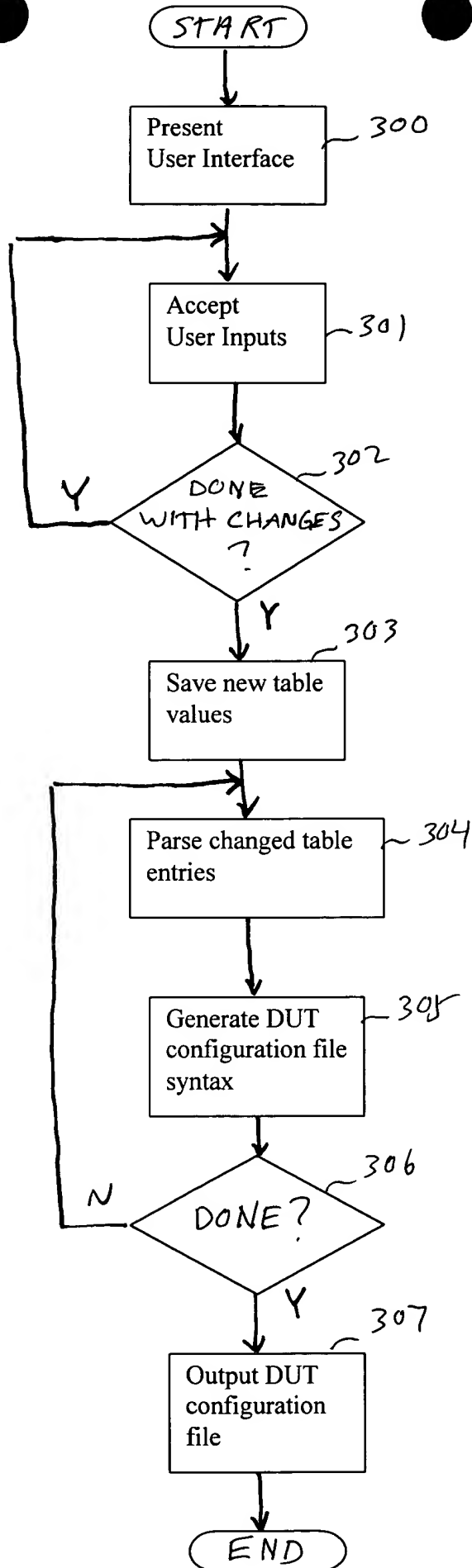


FIG. 3

004480 2528E960

004780 2528950

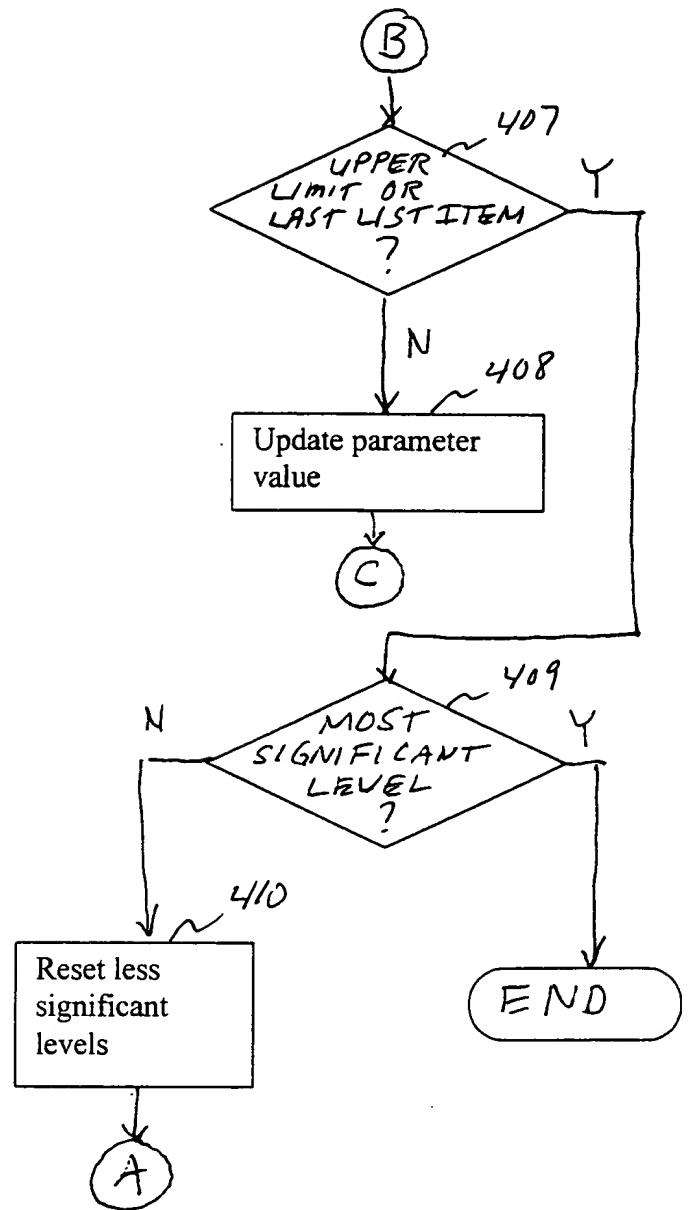
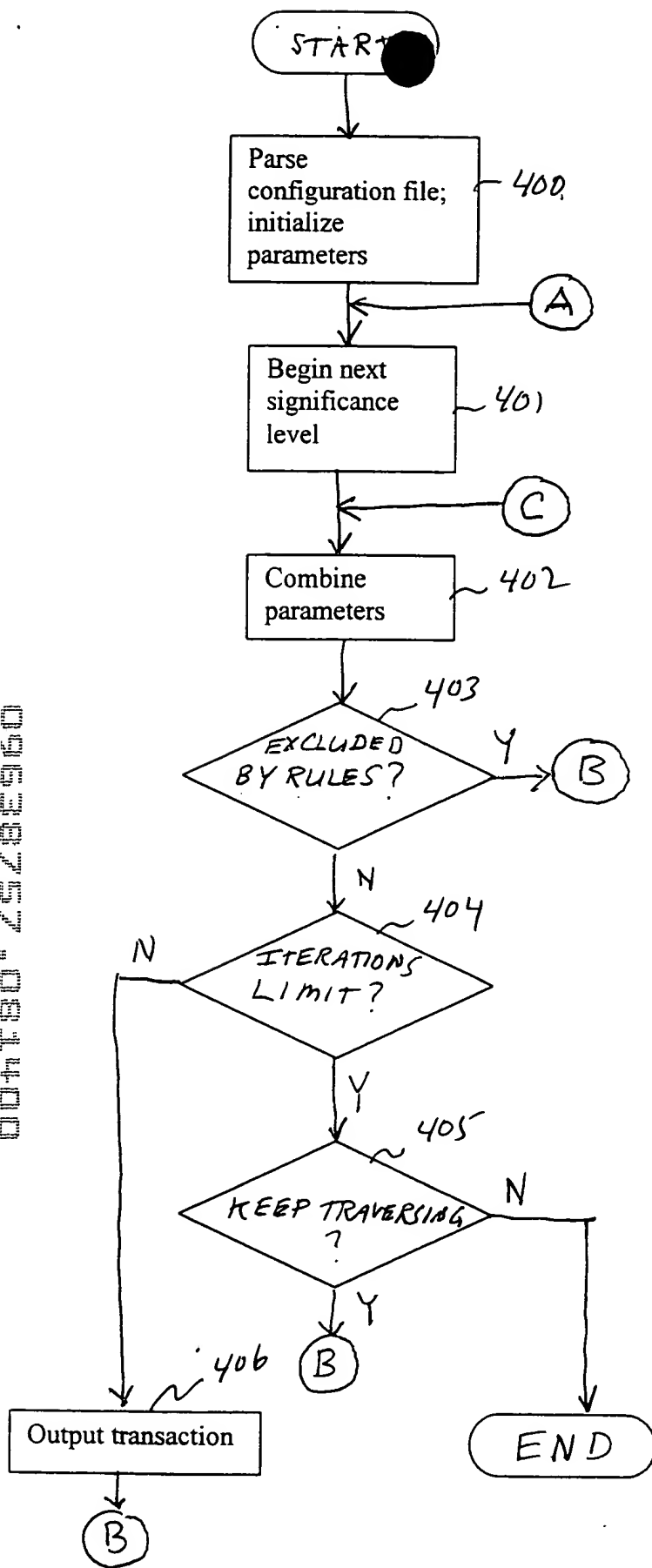


FIG. 4

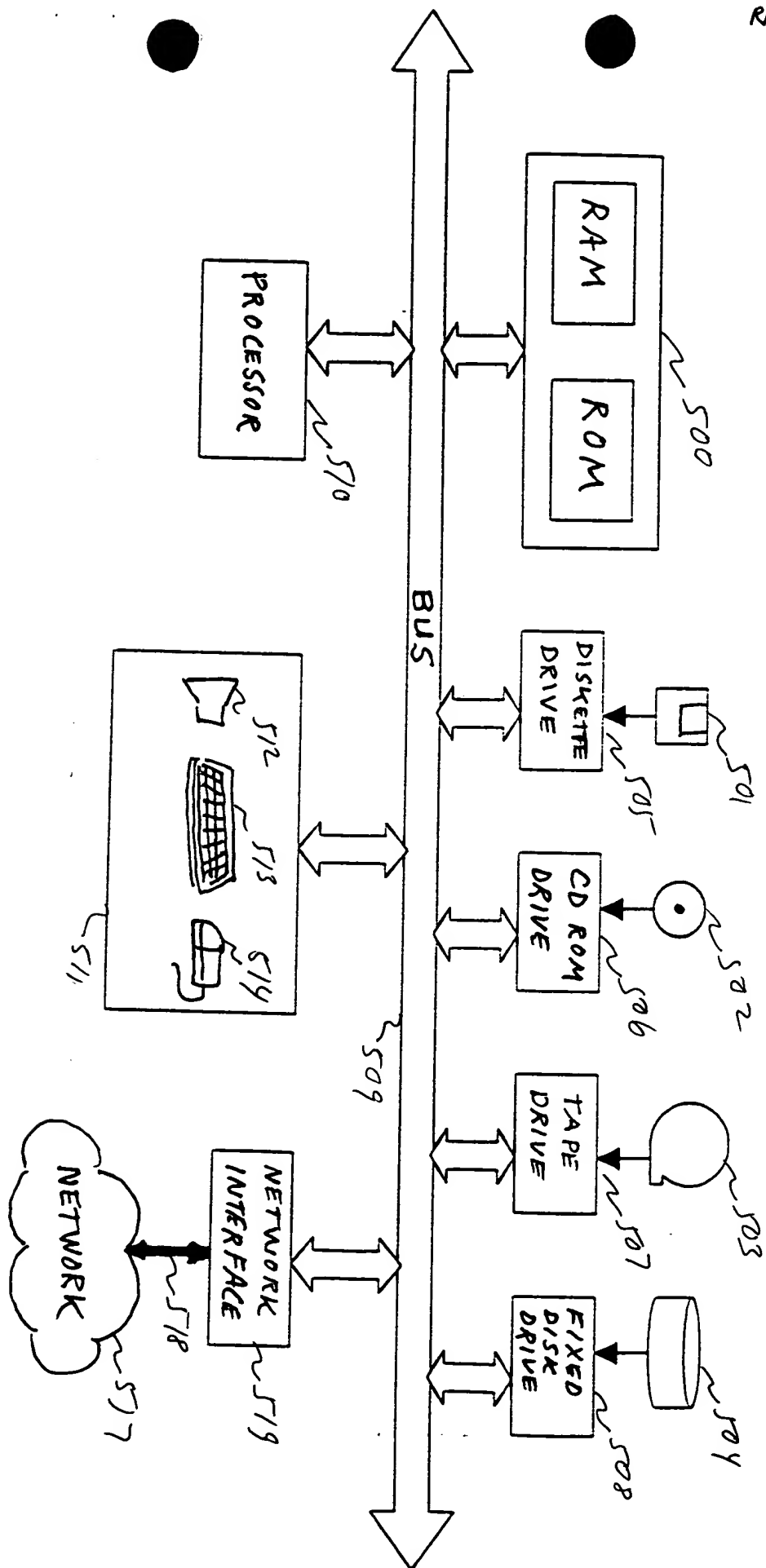


FIG. 5

09638757, 081400